Sierra Components, Inc.

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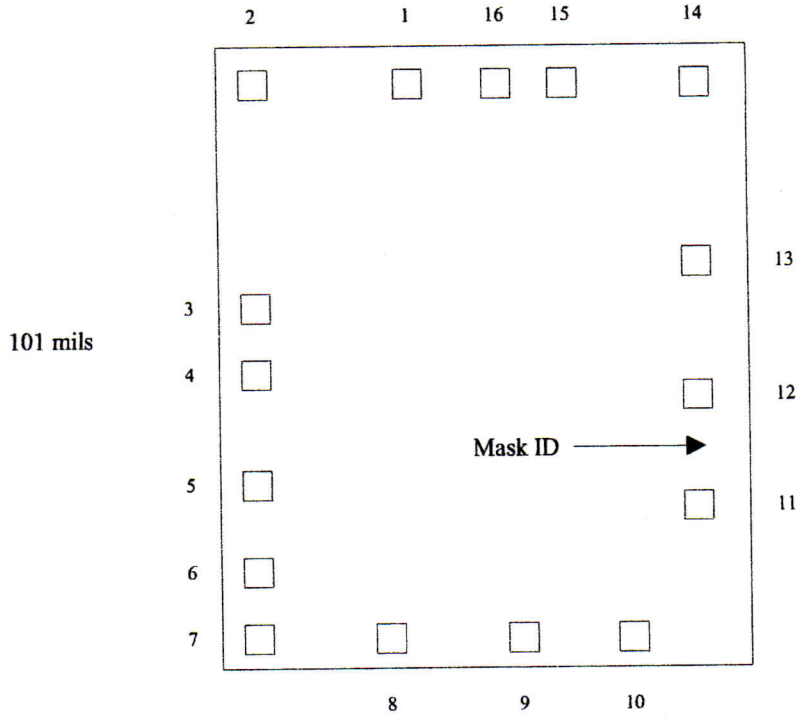
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD	FUNCTION
1	PRESET ENABLE
2	Q4
3	JAM 4
4	JAM 1
5	N. CARRY IN
6	Q1
7	N. CARRY OUT
8	V_{SS}
9	BINARY / DECADE
10	UP / DOWN
11	Q2
12	JAM 2
13	JAM 3
14	Q3
15	CLOCK
16	V_{DD}

Top Material: Al
Backside Material: Si
Bond Pad Size: .004" X .004"
Backside Potential: VDD
Mask Ref: 004116

APPROVED BY: DK	**DIE SIZE .080" X .101"**	**DATE: 4/26/13**
MFG: Texas Inst.	**THICKNESS .025"**	**P/N: CD4029BH**